UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/109,261	06/30/1998	GANG BAI	042390.P5769	3347

7590 09/24/2009

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025

EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

MAIL DATE	DELIVERY MODE
09/24/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GANG BAI

Appeal 2009-010681
Application 09/109,261
Technology Center 2800

Decided: September 24, 2009

Before JOHN C. MARTIN, MAHSHID D. SAADAT,
and ELENI MANTIS MERCADER, *Administrative Patent Judges*.

MANTIS MERCADER, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant seeks our review under 35 U.S.C. § 134(a) of the Examiner's final rejection of claims 8-10, 13-17, 20, and 21. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

INVENTION

Appellant's claimed invention is directed to a transistor gate dielectric having a first dielectric material with a first dielectric constant and a second dielectric material with a second dielectric constant (Spec. 5:2-6).

Claim 8, reproduced below, is representative of the subject matter on appeal:

8. A transistor device having a gate electrode overlying a gate dielectric formed directly on a semiconductor substrate, the gate dielectric comprising:

a first dielectric material selected from the group consisting of HfO_2, BaO, La_2O_3, Y_2O_3, and ZrO_2, and having a first dielectric constant; and

a second dielectric material having a second dielectric constant different from the first dielectric constant,

the first and second dielectric materials being scalable for a set of feature size technologies,

the set of feature size technologies defined by a gate length in the range of 25-70 nm,

wherein the first material thickness and the second material thickness are determined by the relationship

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox},$$

wherein

t_1, is the first material thickness,

t_2, is the second material thickness,

t_{ox}, is the minimum thickness for a gate dielectric of silicon dioxide for a chosen gate length,

k_1, is the dielectric constant for the first dielectric material,
k_2, is the dielectric constant for the second dielectric material, and
k_{ox} is the dielectric constant of silicon dioxide, and

wherein the transistor device is isolated from other devices by shallow trench structures.

THE REJECTION

The Examiner relies upon the following as evidence of unpatentability:

Nagata	US 4,015,281	Mar. 29, 1977
Moon	US 5,621,681	Apr. 15,1997
Momose	US 5,990,516	Nov. 23, 1999 (filed Sep. 13, 1995)

The following rejection is before us for review:

The Examiner rejected claims 8-10, 13-17, 20, and 21 under 35 U.S.C. § 103(a) as unpatentable over Nagata in view of Momose and Moon.

Appellant argues claims 8-9, 13-17, 20, and 21 as a group, with claim 8 as representative (App. Br. 6-8).[1] Accordingly, claims 9, 13-17, 20, and 21 stand or fall with claim 8. *See* 37 C.F.R. § 41.37 (c)(1)(vii) (2004). Claim 10 was separately argued, so we address that claim separately. We note that simply pointing out what a claim requires with no attempt to point out how or why the

[1] Only arguments made by Appellant have been considered in this decision. Arguments which Appellant could have made but did not make in the Brief have not been considered and are deemed waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2004).

claims patentably distinguish over the prior art does not amount to a separate argument for patentability. 37 C.F.R. § 41.37(c)(1)(vii) (2004). *See also In re Nielson*, 816 F.2d 1567, 1572 (Fed. Cir. 1987). Thus, we only address the specific arguments presented, and we do not address Appellant's mere recitation of claim limitations which are without any corresponding argument.

OBVIOUSNESS

ISSUES

Rejection of claims 8-9, 13-17, 20, and 21

Appellant argues that Nagata's equation is not equivalent to the one recited in claim 8 (App. Br.6-7). Appellant further asserts that Nagata does not teach or suggest a transistor device comprising a first dielectric material selected from one of HfO_2, BaO, La_2O_3, Y_2O_3, and ZrO_2 (App. Br. 7).

Appellant asserts that Momose fails to cure the cited deficiencies of Nagata (App. Br. 7). Appellant argues that Momose fails to teach a relationship for material thickness for its dielectric materials according to the claimed equation (App. Br. 7). Appellant argues that Momose's materials do not include those specified for the first dielectric material in claim 8 and the reference does not describe how specific materials are scalable for a set of feature size technologies (App. Br. 7). Appellant asserts that when incorporating Momose into Nagata it does not follow that dielectric materials will have thicknesses determined by the claimed equation (App. Br. 7).

Appellant asserts that while Moon is cited for disclosing specific dielectric materials, Moon does not cure the defects of Nagata and Momose including a gate

dielectric relationship relative to a particular thickness for a gate dielectric silicon dioxide or dielectric materials being scalable for a set of feature size technologies (App. Br. 7).

The Examiner finds that when the $TsiO_2 = 0$, then Nagata's equation becomes the same as Appellant's claimed equation, wherein $Teff/EsiO_2 = (Tx_1/Ex_1 + Tx_2/Ex_2)$, and by substituting for equivalent terminology of the variables, wherein:

$T_{eff} = t_{ox}$

$EsiO_2 = K_{ox}$

$T_{x1} = t_1$

$E_{x1} = k_1$

$T_{x2} = t_2$

$E_{x2} = k_2$, then Nagata's formula becomes: $t_{ox}/ K_{ox} = t_1/k_1 + t_2/k_2$, which is the same as Appellant's claimed equation (Ans. 7). The Examiner explains that Appellant's equation is a simplified form of Nagata's equation which is the standard way of finding the equivalent dielectric thickness of multi-layered dielectric stack (Ans. 7-8).

The Examiner cites Momose to cure the deficiencies of Nagata by teaching a device having a gate length in the range of 25-70 nm (Ans. 8). The Examiner finds that Momose discloses a device having a dual layered gated dielectric and the gate length of the gate electrode being within the desired range (Ans. 9). The Examiner finds that Momose teaches a high performance semiconductor device having low power consumption (col. 16, ll. 28-48 and col. 16, l. 66-col. 17, l. 32), improved

current drive capability (col. 15, ll. 13-31), and improved hot carrier reliability (col. 2, ll. 52-58) (Ans. 9).

The Examiner finds that Moon teaches the specified dielectric materials by teaching Y_2O_3 as a first dielectric and PZT (claims 13 and 20) as a second dielectric forming a good-quality ferroelectric material for the gate dielectric in a semiconductor device (col. 4, ll. 1-12) (Ans. 9).

The issue is whether Appellant has shown that the Examiner erred in finding that the combination of Nagata, Momose, and Moon teaches "a first dielectric material selected from the group consisting of HfO_2, BaO, La_2O_3, Y_2O_3, and ZrO_2;" "a second dielectric material having a second dielectric constant different from the first dielectric constant;" "a gate length of 25-70 nm;" and "wherein the first material thickness and the second material thickness are determined by the relationship $t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$" as recited in claim 8.

Rejection of claim 10

The Examiner finds that Momose teaches the thickness of the gate dielectric is less than one-third the length of the gate because Momose teaches (col. 2, ll. 52-58) as an example that the gate length may be 0.3 micrometers (300 nm) and the insulating film thickness is less than 2.5 nm (Ans. 9). One third of the gate length is 100 nm and obviously, the insulating thickness of 2.5 nm is less than 1/3 the gate length (Ans. 9). The result is that hot carrier problems are reduced (Ans. 9). No matter what the length of the gate, Momose has found that keeping the gate dielectric thin (around 2.5 nm) provides various benefits such as increased current drive capability (col. 15, ll. 10-31) (Ans. 9).

Appellant further argues that Momose teaches that silicon dioxide (a single insulating film) may have a total thickness less than one-third of a length of a transistor gate, not a multi-layer insulating film (App. Br. 8).

The issue is whether Appellant has shown that the Examiner erred in finding that Momose teaches a multi-layer insulating film having a total thickness less than one-third of a length of a transistor gate.

FINDINGS OF FACT

The following findings of fact (FF) supported by a preponderance of the evidence are primarily for emphasis:

1. Moon teaches a semiconductor device having a first dielectric material 11*a* of Y_2O_3, a second dielectric material 12*a* of PZT which has a second dielectric constant, and a gate electrode 13*a* formed over the second dielectric material 12*a* (Fig. 2; col. 4, ll. 1-12; col. 4, ll. 44-55).
2. Moon teaches that the formation of the second dielectric material PZT provides for a good quality ferroelectric film on the semiconductor substrate (col. 4, ll. 10-12).
3. Moon also teaches device isolation area 2 (col. 4, ll. 47-48).
4. Momose teaches a semiconductor device having gate oxide formed of either a silicon oxide film or various other films (col. 16, l. 66-col. 17, l. 32) in which the feature size technology has a gate length of 0.15 μm (150 nm) (col. 16, ll. 29-48) to form a high performance semiconductor having a low power consumption (col. 17, ll. 30-32).

5. Momose further teaches that the gate length can be decreased even more to improve the current drive capability (col. 15, ll. 13-31), wherein a gate length of 0.04 μm (40 nm) (col. 15, ll. 25-31) improved the current drive capability by 20 to 30 % (col. 15, ll. 25-31).
6. Nagata teaches the equation for determining thickness of a layer in a multi-layer film or double layer film (col. 4, ll. 34-44).
7. Nagata's equation is based on the "effective oxide thickness" T_{eff} which is the film thickness as calculated in terms of a single-layer film of SiO_2 (col. 4, ll. 32-34) and the dielectric constant of SiO_2 (col. 4, ll. 45-46).
8. The Examiner finds that Momose teaches the thickness of the gate dielectric is less than one-third the length of the gate because Momose teaches (col. 2, ll. 52-58) as an example that the gate length may be 0.3 micrometers (300 nm) and the insulating film thickness is less than 2.5 nm (Ans. 9).
9. The Examiner also finds that one third of the gate length is 100 nm and obviously, the insulating thickness of 2.5 nm is less than 1/3 the gate length (Ans. 9).
10. It is uncontested that Momose teaches that silicon dioxide (a single insulating film) has a total thickness less than one-third of a length of a transistor gate (App. Br. 8).
11. Momose makes clear that while the discussion focused on silicon dioxide (a single insulating film) also various other films (i.e., multi-layered insulating) can be used instead (col. 16, l. 66-col. 17, l. 32).

PRINCIPLES OF LAW

The Examiner bears the initial burden of presenting a prima facie case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). If that burden is met, then the burden shifts to the Appellants to overcome the prima facie case with argument and/or evidence. *Id.*

"[O]ne cannot show non-obviousness by attacking references individually where . . . the rejections are based on combinations of references." *In re Keller*, 642 F.2d 413, 425 (CCPA 1981).

"The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference …. Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." *Id.* at 425.

When a rejection is based on a combination of references, the order in which prior art references are cited to the Applicant is of no significance, but merely a matter of exposition. *In re Bush*, 296 F. 2d 491, 496 (CCPA 1961).

ANALYSIS

Rejection of claims 8-9, 13-17, 20, and 21

Moon teaches a semiconductor device having a first dielectric material 11*a* of Y_2O_3, a second dielectric material 12*a* of PZT which has a second dielectric constant, and a gate electrode 13*a* formed over the second dielectric material 12*a* (FF 1). The formation of the second dielectric material PZT provides for a good quality ferroelectric film on the semiconductor substrate (FF 2). Moon also teaches "a first dielectric material selected from the group consisting of HfO_2,

BaO, La_2O_3, Y_2O_3, and ZrO_2" (i.e., Y_2O_3) and "a second dielectric material having a second dielectric constant different from the first dielectric constant" (i.e., PZT). Moon also teaches device isolation area 2 (i.e., shallow trench structures) (FF 3). Moon does not teach a gate length in the range of 25-70 nm.

Momose teaches a semiconductor device having either a silicon oxide film or one of various other films in which the feature size technology has a gate length of 0.15 μm (150 nm) to form a high performance semiconductor having a low power consumption (FF 4). Momose further teaches that the gate length can be decreased even more to improve the current drive capability, wherein a gate length of 0.04 μm (40 nm) improved the current drive capability by 20 to 30 % (FF 5). Thus, Momose teaches "a gate length of 25-70 nm" (i.e., 40 nm). Accordingly, one skilled in the art would be motivated to modify Moon with the gate length of 40 nm as taught by Momose to improve the current drive capability.

Furthermore, Nagata teaches the equation for determining thickness of a layer in a multi-layer film or double layer film (FF 6).

This equation is in terms of the "effective oxide thickness" T_{eff} which is the film thickness as calculated in terms of a single-layer film of SiO_2 and the dielectric constant of SiO_2 (FF 7).

The listed equation is:

$$T_{eff} = (TSiO_2/ESiO_2 + Tx_1/Ex_1 + Tx_2/Ex_2 + Tx_3/Ex_3 \ldots + Tx_n/Ex_n)\ ESiO_2$$

Wherein the Tx_i and Ex_i (i= 1, 2, . . . i, n) are the thickness and dielectric constant of the films other than SiO_2.

Accordingly, one skilled in the art would know to use this equation in Moon to determine the thickness of the first dielectric material (i.e., Y_2O_3) and the second dielectric material (i.e., PZT).

The equation above can be re-written as:

$T_{eff} / ESiO_2 = (TSiO_2/ESiO_2 + Tx_1/Ex_1 + Tx_2/Ex_2 + Tx_3/Ex_3 \ldots + Tx_n/Ex_n)$

Since Moon only teaches using the dielectric materials of Y_2O_3 and PZT without a SiO_2 layer, the term $TSiO_2/ESiO_2$ will be equal to zero and the equation becomes:

$T_{eff} / ESiO_2 = (0 + Tx_1/Ex_1$ (i.e., for Y_2O_3) $+ Tx_2/Ex_2$ (i.e., for PZT)).

Note that this is the same equation as recited in claim 8 and described as equation (4) in Appellant's Specification (Spec. 10) of $t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$

wherein

t_1, is the first material thickness (i.e., Tx_1),

t_2, is the second material thickness (i.e., Tx_2),

t_{ox}, is the minimum thickness for a gate dielectric of silicon dioxide for a chosen gate length (i.e., T_{eff}),

k_1, is the dielectric constant for the first dielectric material (i.e., Ex_1),

k_2, is the dielectric constant for the second dielectric material (i.e., Ex_2), and

k_{ox} is the dielectric constant of silicon dioxide (i.e., $ESiO_2$).

Thus, one skilled in the art would know how to use the above equation as taught by Momose to determine the thickness of the dielectric layers in Moon.

Accordingly, we are not persuaded by Appellant's arguments (App. Br. 6-8), because the arguments attack the references individually where the rejection was

based on the combination of the reference. *See Keller*, 642 F.2d at 425. We further note that when a rejection is based on a combination of references, the order in which prior art references are cited to the Appellant is of no significance, but merely a matter of exposition. *See Bush*, 296 F. 2d at 496.

For the foregoing reasons, we sustain the rejection of claim 8 and claims 9, 13-17, 20, and 21, which fall with claim 8.

Rejection of claim 10

The Examiner finds, and we agree, that Momose's thickness of the gate dielectric is less than one-third the length of the gate because Momose teaches as an example that the gate length may be 0.3 micrometers (300 nm) and the insulating film thickness is less than 2.5 nm (FF 8). The Examiner also finds that one third of the gate length is 100 nm and obviously, the insulating thickness of 2.5 nm is less than 1/3 the gate length (FF 9). Furthermore, it is uncontested that Momose teaches that silicon dioxide (a single insulating film) has a total thickness less than one-third of a length of a transistor gate (FF 10). The pivotal issue is whether this thickness ratio extends to a multi-layer insulating film.

Momose makes it clear that while the discussion focused on silicon dioxide (a single insulating film) also various other films (i.e., multi-layered insulating) can be used instead (FF 11).

For the foregoing reasons, we also sustain the rejection of claim 10.

CONCLUSIONS

Under 35 U.S.C. § 103, Appellant has not shown that the Examiner erred in finding that the combination of Nagata, Momose, and Moon teaches "a first dielectric material selected from the group consisting of HfO_2, BaO, La_2O_3, Y_2O_3, and ZrO_2;" "a second dielectric material having a second dielectric constant different from the first dielectric constant;" "a gate length of 25-70 nm;" and "wherein the first material thickness and the second material thickness are determined by the relationship $t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$."

Appellant has also not shown that the Examiner erred in finding that Momose teaches a multi-layer insulating film having a total thickness less than one-third of a length of a transistor gate.

ORDER

The decision of the Examiner to reject claims 8-10, 13-17, 20, and 21 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

ELD

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025